REMARKS

This responds to the Office Action dated on August 18, 2006.

Objection to the Claims

Claims 1, 12, 22 and 23 were objected to under 35 U.S.C. 132(a). The Examiner stated in his objection that the amendment to the claims filed June 5, 2006 introduces new matter into the disclosure.

As noted by the Examiner, the amendment to claims 1, 12, 22 and 23 adds the limitation "wherein transfer of data associated with the memory request occurs independently of the processor that generated the communication request." The Examiner stated that Applicant introduced new matter into the disclosure when this amendment was entered.

Applicant respectfully disagrees.

As noted in the specification at p. 3, lines 17-19, "there is a need for a node translation mechanism for communicating over virtual channels in a clustered system that supports user-level communications without the need for OS intervention on communication events." The acronym OS stands for "operating system". To accomplish this, each SHUB (SHUB 30 in Fig. 2) includes a communication engine (CE 64 in Fig. 3) that is "capable of performing user-level block transfers." Specification, p. 9, lines 12-14.

> CE 64 is capable of performing user-level block transfers and AMOs both within and between coherence domains using the same user-level software interface. In particular, CE 64 includes a plurality of memory-mapped registers (MMRs) which can be programmed by user processes running in processor 24A or 26A to perform block transfers or AMOs. CE 64 can be programmed to function as a block transfer engine to transfer blocks of data (immediate data, or data stored within a source memory buffer) by generating coherence protocol requests (i.e., "PUTs" and "GETs") that blast data into memory in a coherence snapshot without the need to first obtain a shared copy of the data. The data can be moved from local memory to local memory, from local memory to remote memory, from remote memory to local memory, and from remote memory to remote memory.

Specification, p. 9, lines 15-25. In addition, Applicant states that, "due to the address translation mechanism described below, CE 64 can advantageously be directly programmed by user

processes using virtual addresses, and can operate without operating system (OS) intervention after initial set up." Specification, p. 9, line 27 through p. 10, line 1.

One of skill in the art would realize when reading this section that "transfer of data associated with the memory request occurs independently of the processor that generated the communication request." A more detailed set of examples is set out at p. 27, line 15 through p. 29, line 11.

As a side note, the sections cited by the Examiner relate to the operation of physical communication interfaces (CIs) within a CE 64 within a SHUB 30. There are a number of physical communication interfaces (CIs) within each CE. Both the CIs and the CEs are, however, part of the SHUB and, therefore, are separate from the processors (as can be seen in Fig. 2).

Applicant respectfully submits that the limitation added June 5, 2006 merely describes a feature of the invention that was present and described when the application was filed. Reconsideration is respectfully requested.

§103 Rejection of the Claims

Claims 1-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,649,141) in view of Mazzola et al. (U.S. Patent No. 5,740,171).

Rejections under U.S.C. § 103

1) The Applicable Law

According to *M.P.E.P.* § 2141, which cites *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986), the following tenets of patent law must be adhered to when applying 35 U.S.C. § 103. First, the claimed invention must be considered as a whole. Second, the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination. Third, the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention. Fourth, obviousness is determined using a reasonable expectation of success standard. Under § 103, the scope and content of the prior art are to be determined; differences between the prior art

and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. *M.P.E.P.* § 2141 (citing *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966)).

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d, 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellants' disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). The references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references. *M.P.E.P.* § 2142 (citing *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)). In considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw there from. *M.P.E.P.* § 2144.01 (citing *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968)). However, if the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *M.P.E.P.* § 2143.01 (citing *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)).

In order to take into account the inferences which one skilled in the art would reasonably make, the examiner must ascertain what would have been obvious to one of ordinary skill in the art at the time the invention was made. *M.P.E.P.* § 2141.03 (citing *Environmental Designs, Ltd. v. Union Oil Co*, 713 F.2d 693, 218 USPQ 865 (Fed. Cir. 1983), *cert. denied*, 464 U.S. 1043 (1984)).

> The examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. Knowledge of Appellants' disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the "differences," conduct the search and evaluate the "subject matter as a whole" of the invention. The tendency to resort to "hindsight" based upon Appellants' disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

M.P.E.P. § 2141.03.

2) Application of §103 to the Rejected Claims

Claims 1-27 were rejected under 35 USC § 103(a)

Claims 1-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,649,141) in view of Mazzola et al. (U.S. Patent No. 5,740,171).

Yamazaki describes a memory translation mechanism that converts an address having a virtual cluster designation into an intermediate address having a physical cluster designation. The physical cluster designation is then used to route the memory request.

Mazzola describes a forwarding engine used within a switch. The forwarding engine accepts a frame, examines a portion of the header contents to determine the destination of the data and generates a unique index for each frame in response to the frame's "color" and destination address. "In order to generate this index, the EARL employs a novel address translation mechanism that essentially maps the frame's destination address and color (DA/color) to a destination port using forwarding tables; as described herein, the tables contain, inter alia, a unique index value assigned to each port in the switch." Therefore, the "address translation" is for determining the port within the switch to use when forwarding the frame.

The Examiner stated that Yamazaki discloses each of the limitations of claims 1, 12, and 22-24 but one, stating that Yamazaki fails to disclose a connection descriptor for a virtual connection. The Examiner then states that Mazzola discloses accessing a local connection table

using a connection descriptor of the forwarding tables to produce a system node identifier for the endpoint node. Applicant respectfully disagrees.

Claims 1 and 12 require that the method permits indirect addressing of endpoint nodes. To accomplish this the method requires "assigning a connection description to a virtual connection, the connection descriptor being a handle that specifies an endpoint node for the virtual connection," "defining a local connection table accessible by the communication engine, wherein the local connection table is configured to be accessed using the connection descriptor to produce a system node identifier for the endpoint node," and "in response to the communication request, accessing, via the communication engine, the local connection table using the connection descriptor of the communication request to produce the system node identifier for the endpoint node for the virtual connection." Claims 22 and 23 have corresponding limitations in their system claims.

As noted by the Examiner, Yamazaki fails to disclose assigning a connection descriptor for a virtual connection. Applicant respectfully submits that Yamazaki also fails to disclose a communication engine as defined and claimed by Applicant and a local connection table accessible by the communication engine as defined and claimed by Applicant. Instead, the Examiner points to a virtual-to-physical cluster translation table 130 used to translate "a logical cluster number contained in [the] virtual address into a physical cluster number corresponding thereto." In order to operate, the virtual address according to Yamazaki must include a logical cluster number that can be used to access the cluster translation table. In contrast, as noted at p. 26, lines 9-10, Applicant generates both a virtual address and a connection description. The connection description is used to access the local connection table in order to generate a system node identifier (SNID) that is then used to route the virtual address. Such an approach is much more flexible than that described by Yamazaki since the full address field can be used to access memory and memory mapped registers at the remote node.

Furthermore, Yamazaki fails to show that "transfer of data associated with the memory request occurs independently of the processor that generated the communication request" as described by Applicant and claimed in claims 1-27. Such an approach is enabled through the use of the multiple communication interfaces within each communication engine. There is no such mechanism in any of the references cited by the Examiner.

Finally, as noted above, there is no teaching within Mazzola of using a connection descriptor to produce a system node identifier as described and claimed by Applicant.

With regard to claims 5, 6, 9, 16, 17 and 20, the Examiner stated that, although Yamazaki fails to disclose "a key for qualifying an address translation at the endpoint node," Mazzola shows such a key. Applicant describes the key at p. 12, line 27 through p. 13, line 3, as an address space number (ASN) used to translate its corresponding virtual address.

The section in Mazzola cited by the Examiner describes calculating a key used to select a destination port of a router. The key is a hash of the 48-bit media access control (MAC) address and a 10-bit color identifier. The translation that Mazzola describes is the hash transformation of the 58-bit combination of the MAC address and the 10-bit color identifier. The key is never used to "qualifying an address translation at the endpoint node" as required by each of claims 5, 6, 9, 16, 17 and 20.

Applicant respectfully submits that none of the cited references describe or suggest each of the limitations of claims 1-27. Applicant respectfully requests reconsideration and allowance of claims 1-27.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

STEVEN L. SCOTT (DO NOT USE) ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6909

Date Nov. 10, 2006

By Thomas J. Brennan
Thomas F. Brennan
Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 10 day of November 2006.

Lisa Rossbach
Name

Lisa Rossbach
Signature